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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,739	01/16/2002	Matthew M. Borg	10010697	8645

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EXAMINER	
QUIETT, CARRAMAH J	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/051,739	BORG, MATTHEW M.	
	Examiner	Art Unit	
	Carramah J. Quiett	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02072005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS), filed on 01/16/2002, has been placed in the application file, and the information referred to therein has been considered as to the merits.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: In the specification (page 12, lines 18-19), Applicant states that a source terminal of the FET M2 is coupled to a drain terminal of a third FET M3. However, one of the limitations in claim 6, "a drain terminal coupled to a drain terminal of the second FET," does not agreed with the disclosure. Instead, that limitation should be, "a *drain* terminal coupled to a *source* terminal of second FET." – this is how the Examiner will consider that limitation in claim 6.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-3 and 5-14** are rejected under 35 U.S.C. 102(e) as being anticipated by Fowler (U.S. Pat. #6,424,375).

For **claim 1**, Fowler discloses an image capture system (fig. 1) comprising,

- a pixel (100) comprising:
  - a first FET (108) having a gate terminal (109) coupled to a reset line for providing a reset signal (col. 3, lines 55-58; col. 4, lines 20-22 and 31-34), a drain terminal (113) coupled to a supply voltage (V_{dd}; col. 4, 25-27), and a source terminal (111); and
  - a photodetector coupled (112) between a first ground and the source terminal of the first FET (fig. 1; col. 4, lines 22-25);
- a first switching device (122) selectively coupled to the reset line (col. 4, lines 30-34); and
- a reference voltage source (V_{pr}) coupled between a second ground and the reset line via the first switching device (col. 4, lines 7-19), wherein the reference voltage source generates a ground referenced reset voltage (V_g; col. 4, lines 15-19) and the first and second grounds have the same potential (col. 7, line 61-66).

For **claim 2**, Fowler further discloses an image capture system comprising an operational amplifier buffer (106) coupled between the reset line and the reference voltage source (col. 3, lines 58-60; col. 4, lines 20-22).

For **claim 3**, Fowler further discloses an image capture system wherein the first FET further comprises an n-channel enhancement mode MOSFET (col. 3, line 60).

For **claim 5**, Fowler further discloses an image capture system comprising a second FET (114) having a gate terminal coupled to the source terminal of the first FET and a drain terminal coupled to the supply voltage. As shown in circuits 102 and 104 of fig. 1, the drain terminal of second FET (114) is connected to the supply voltage, V_{dd}, and the gate terminal is connected to the first FET (108) via a node (110). Also read col. 3, lines 39-43.

For **claim 6**, Fowler further discloses an image capture system comprising a third FET (116) having a gate terminal coupled to a row select line, a source terminal coupled to a column line, and a drain terminal coupled to a source terminal of the second FET. See figure1 and read col. 3, lines 39-43. The pixel of Fowler is a typical CMOS Active Pixel Sensor (APS) (col. 3,lines 21-54). Therefore, it is inherent for the transistor (116) to have a row select line at the gate terminal and a column line at the source terminal.

For **claim 7**, Fowler discloses an apparatus (fig. 1) comprising:

- a pixel having a photodetector (112) coupled to a reset transistor, the reset transistor (108) being configured to receive a reset signal (col. 3, lines 55-58; col. 4, lines 20-22 and 31-34);
- a reference voltage source (V_{pr}) coupled to the reset transistor for providing the reset signal to the reset transistor (col. 4, lines7-19); and
- a supply voltage source (V_{dd}) coupled to the reset transistor for resetting the photodetector between exposure intervals (col. 4, lines 50-67).

For **claim 8**, Fowler further discloses an apparatus wherein the photodetector and the reference voltage source are each grounded to a common potential (col. 7, line 61-66).

For **claim 9**, Fowler further discloses an apparatus wherein the photodetector is grounded at a ground voltage and the reset signal is equal to the reference voltage or the reference voltage plus a boost level when the reset signal is asserted high and is equal to the ground voltage when asserted low (col. 4, lines 50-67).

For **claim 10**, Fowler further discloses an apparatus wherein the reset transistor comprises an n-channel enhancement mode MOSFET (col. 3, line 60).

For **claim 11**, Fowler further discloses an apparatus wherein the reset transistor comprises an n-channel enhancement mode MOSFET having a gate terminal coupled to the reference voltage source (col. 3, lines 55-58; col. 4, lines 20-22 and 31-34), a drain terminal coupled to the supply voltage (V_{dd}; col. 4, 25-27), and a source terminal (111) coupled to the photodetector (fig. 1; col. 4, lines 22-25).

For **claim 12**, Fowler further discloses an apparatus wherein the photodetector (112/ col. col. 4, lines 22-25) comprises a photodiode (col. 4, line 67).

For **claim 13**, Fowler further discloses an apparatus comprising a switching device (compare module 106 and switch 122) coupled between the reference voltage source and the reset transistor (col. 4, lines 20-22; col. 4, lines 31-34).

For **claim 14**, Fowler discloses an apparatus wherein the switching device (fig. 1, refs. 106 and 122) comprises a multiplexer. The compare module (106) and the switch (122) receive signals from V_r, V_{pr}, or V_g, and the output of V_2 to reset transistor (108). Therefore, the compare module (106) and the switch (122) inherently multiplex signals from V_r, V_{pr}, and V_g.

5. **Claims 15-20** are rejected under 35 U.S.C. 102(b) as being anticipated by Dhuse et al. (U.S. Pat. #6,133,862).

For **claim 15**, Dhuse discloses a method comprising:

- providing a first reset (V_{reset1}) signal to a pixel, the first reset signal being equal to a reference voltage (col. 7, lines 46-51);
- resetting the pixel in response to the first reset signal (V_{reset1}) using a supply voltage, the supply voltage being different from the reference voltage;

  In col. 7, lines 45-51, Dhuse teaches that the sensor array is reset to a value of V_{reset}, which is approximately the supply voltage (V_{reset} approximately V_{cc}-V_{TM1}; col. 5, line 19 – 24);
- reading a first voltage value generated at the pixel following a light exposure interval (col. 5, line 57 – col. 6, line 1);
- providing a second reset signal (V_{reset2}) to the pixel, the second reset signal being equal to the reference voltage (col. 7, lines 54-56);
- reading a second voltage value from the pixel (col. 7, lines 56-59); and
- generating a pixel value using the first and the second voltage values (col. 7, lines 51-54 and 59-67).

For **claim 16**, Dhuse further discloses a method wherein the pixel value equals the second voltage value minus the first voltage value (col. 7, lines 59-66).

For **claim 17**, Dhuse further discloses a method wherein the first voltage value is approximately proportional to a light intensity detected by the pixel during the light exposure interval (col. 5, line 57 – col. 6, line 9).

For **claim 18**, Dhuse further discloses a method comprising repeating the providing a first reset signal to a pixel, reading a first voltage value, providing a second reset signal to the pixel, reading, and generating for a plurality of pixels (col. 7, lines 45-67).

For **claim 19**, Dhuse further discloses a method wherein the generating is performed by a column circuit (col. 7, lines 10-35).

For **claim 20**, Dhuse further discloses a method wherein the reading a first voltage value comprises exposing a photodiode to incident light (col. 4, lines 7-22).

6. **Claims 1 and 4** are rejected under 35 U.S.C. 102(b) as being anticipated by Borg (U.S. Pat. #6,147,846).

For **claim 1**, Borg discloses an image capture system (fig. 2) comprising,

- a pixel (110) comprising:
  - a first FET (112, which is analogous to the prior art transistor [fig. 1, ref. 12]) having a gate terminal coupled to a reset line for providing a reset signal (col. 1, line 28), a drain terminal coupled to a supply voltage (V_{DD}; col. 1, lines 26-27), and a source terminal (see figs. 1 and 2; col. 1, lines 15-29); and
  - a photodetector coupled (see fig. 2, not numbered) between a first ground and the source terminal of the first FET (see fig. 2; col. 1, lines 15-29);
- a first switching device (150) selectively coupled to the reset line (fig. 2; col. 3, lines 21-39); and
- a reference voltage source (152) coupled between a second ground and the reset line via the first switching device (col. 3, lines 29-39), wherein the reference voltage

source generates a ground referenced reset voltage (Row Reset; col. 3, lines 40-65) and the first and second grounds have the same potential (col. 3, lines 29-39).

For **claim 4**, Borg further discloses an image capture system wherein the ground referenced reset voltage is greater than the supply voltage (col. 3, lines 40-65). When the DRV switch is closed, the INT switch, and the RSTB is driven low, the ROW RESET (containing ground, referenced, and reset voltages) is driven low, which further drives the row reset signal above the supply voltage using the equation (1) on col. 3, line 64.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fossum et al. (U.S. Pat. #5,471,515) An active pixel sensor comprising 3-FETs. The reset FET has a drain connected to the voltage supply.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carramah J. Quiett whose telephone number is (703) 305-0566. The examiner can normally be reached on 8:00-5:00 M-F. *Beginning March 2005, the examiner's telephone number will be changed to (571) 272-7316.*

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.J.Q.
Feb. 7, 2005

NGOC-YEN VU
PRIMARY EXAMINER